EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claims 49 and 84-87 are cancelled as being drawn to nonelected groups, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/04/2010.

Authorization for this examiner's amendment was given in a telephone interview with Jeffrey R. Filipek on 06/24/2010.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Claim 63 is amended as follows:

63. A digital signal receiving device which is adapted to receive a digital communication signal, has a function of generating a clock signal based on PCR data included in the communication signal, and has a function of transmitting a stream signal in the form of a plurality of packets, as well as the clock signal, the stream signal including the communication signal, the digital signal receiving device being configured so as to establish a digital signal receiving system by being interconnected via an interface section to a host device which is

adapted to receive the stream signal and the clock signal from the digital signal receiving device via the interface section, the digital signal receiving device comprising: a recipient STC counter which counts the number of clocks of the clock signal, and outputs the counter value as recipient STC data; a variation detector which calculates a difference between the recipient STC data and the PCR data as difference data, and detects a variation in frequency of the clock signal that exceeds a predetermined value based on the difference data; and a variation processor which sends, to the host device, variation information data obtained based on the recipient STC data and the PCR data, and sets the PCR data in the recipient STC counter if the variation detector detects that the variation in frequency that exceeds the predetermined value.~~"~~ , and the host device including: a host STC counter which counts the number of clocks of the clock signal sent from the digital signal receiving device, and outputs the counter value as host STC data; and an STC correcting unit which calculates correction data based on the host STC data and the variation information data if the variation detector detects the variation in frequency that exceeds the predetermined value, and sets the correction data in the host STC counter so as to coincide the counter value set in the recipient STC counter with the counter value set in the host STC counter.

Reasons for allowance

3. The following is an examiner's statement of reasons for allowance:

The present invention is directed to a digital signal receiving system and device provided for establishing high speed clock resynchronization. The independent claims identify the uniquely distinct feature "a variation processor which sends, to the host device, variation information data obtained based on the recipient STC data and the PCR data, and sets the PCR

data in the recipient STC counter if the variation detector detects that the variation in frequency that exceeds the predetermined value, and the host device including: a host STC counter which counts the number of clocks of the clock signal sent from the digital signal receiving device, and outputs the counter value as host STC data; and an STC correcting unit which calculates correction data based on the host STC data and the variation information data if the variation detector detects the variation in frequency that exceeds the predetermined value, and sets the correction data in the host STC counter so as to coincide the counter value set in the recipient STC counter with the counter value set in the host STC counter." The closest prior arts, Demas (US PG PUB 2005/0175322), Seo (US PG PUB 2004/0165867), Ishioka (US PG PUB 2004/0055013), Nagata (US PG PUB 2002/0076196), Jang (US Pat. No. 7,705,652), Inazumi (US Pat. No. 6, 731,658), Honma (US Pat. No. 5, 923, 220), either singularly or in combination fail to anticipate or render the above limitation obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELEN SHIBRU whose telephone number is (571)272-7329. The examiner can normally be reached on M-F, 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, THAI Q. TRAN can be reached on (571) 272-7382. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HELEN SHIBRU/
Examiner, Art Unit 2621
June 30, 2010

/Thai Tran/
Supervisory Patent Examiner, Art Unit 2621